REMARKS

Claims 1-7, 9-14 and 16-24 are pending in this application. Claim 1 has been amended. No new matter has been introduced.

Claims 1-7, 9-14 and 16-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chen et al. (U.S. Patent No. 5,482,881) ("Chen") in view of Gardner et al. (U.S. Patent No. 6,127,235) ("Gardner"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming source pockets on a substrate which may be employed, as recited in some claims, in a flash memory. As such, amended independent claim 1 recites a "method of forming a plurality of dopant pockets on a substrate" by *inter alia* "forming a plurality of implantable regions on said substrate separated by field oxide regions" and "forming a plurality of word lines located over said implantable regions and field oxide regions." Amended independent claim 1 also recites "removing portions of said field oxide regions between two adjacent word lines to expose respective substrate regions" and "forming source regions of a first conductivity type in said implantable regions." Amended independent claim 1 further recites "subsequently implanting a dopant of a second conductivity type which is different from said first conductivity type into said substrate through said respective substrate regions to form said dopant pockets beneath said source regions."

Independent claim 12 recites a "method of forming a plurality of dopant pockets on a substrate" by *inter alia* "forming a plurality of implantable regions on said substrate separated by field oxide regions, said implantable regions and field oxide regions extending in a first direction" and "forming a plurality of word lines located over said implantable regions and field oxide regions, said word lines extending in a second direction perpendicular to said first direction." Independent claim 12 also recites "implanting a dopant into said substrate through said respective substrate regions to form said dopant pockets beneath said source regions, said photoresist operating as a mask for forming said source regions and said dopant pockets, wherein said act of implanting said dopant into said substrate is carried out before said act of forming said source regions."

Independent claim 19 recites a "method of forming source regions with boron pockets on a substrate of a flash memory" by *inter alia* "forming a pair of adjacent spaced word lines" and "forming a layer of photoresist over . . . said word lines." Independent claim 19 also recites the steps of "patterning said photoresist to expose a portion of said field oxide layer located between said word lines" and "implanting boron into said substrate in between said word lines to form a boron pocket beneath said source region, said photoresist operating as a mask for forming said source region and said boron pocket, wherein the act of implanting boron into said substrate is carried out before said act of forming said source region."

Independent claim 24 recites a "method of forming a source region in a substrate" by *inter alia* "forming a pair of gate structures which extend in a first direction over a substrate" and "providing a layer of photoresist over said pair of gate structures." Independent claim 24 also recites "providing a second doped layer in said substrate between said pair of gate structures which is below said first doped layer and which has a profile which follows that of said first doped layer, said photoresist operating as a mask for providing said first doped layer and said second doped layer, wherein said act of providing said second doped layer is carried out with an implanting energy higher than an implanting energy for said first doped layer and wherein said second doped layer is provided in said substrate before said first doped layer."

Chen relates to a "flash EEPROM having reduced column leakage current." (Abstract). Chen teaches that "[S]ource 112 and drain 114 regions . . . are conventionally formed by initially implanting n-type dopants with a conventional double diffusion implant (DDI) . . . to form a deeply diffused but lightly doped N well 130." (Col. 6, lines 55-63; Figures 1 and 4B). Chen also teaches that "[A] shallow second implant, commonly referred to as a medium diffused drain (MDD) implant, is then performed (e.g. with arsenic) . . . to create a more heavily doped, but shallower, n+ well 132 embedded within deep N well 130." (Col. 6, lines 55-63; Col. 7, lines 1-5; Figures 1, 4B, 4D).

Gardner relates to a semiconductor device having a "gate with a first material having a first dielectric constant adjacent the semiconductor substrate and a second

material having a second dielectric constant adjacent the semiconductor substrate." (Abstract). Gardner teaches that a "conductor, such as polysilicon, is then placed on the gate so that the first and second materials are sandwiched between the conductor and the semiconductor substrate." (Abstract). In this manner, "[s]ince the dielectric constants of the two materials are different, the gate acts like a gate having a single dielectric with at least two thicknesses." (Abstract).

The subject matter of claims 1-7, 9-14 and 16-24 would not have been obvious over Chen in view of Gardner. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996).

In the present case, Chen and Gardner, whether considered alone or in combination, fail to teach or suggest all limitations of the claimed invention. First, neither Chen nor Gardner teaches or suggests all limitations of independent claim 1. Chen does not teach or suggest "forming source regions of a first conductivity type in said implantable regions" and "subsequently implanting a dopant of a second conductivity type which is different from said first conductivity type into said substrate through said respective substrate regions to form said dopant pockets beneath said source regions," as amended independent claim 1 recites. Chen teaches that the source region 112 is formed by "initially implanting n-type dopants with a conventional double diffusion implant (DDI) to form a deeply diffused but lightly doped N well 130" and then conducting "[a] shallow second implant . . . to create a more heavily doped, but shallower, n+ well 132 embedded within deep N well 130." (Col. 6, lines 55-63; Col. 7, lines 1-5; Figures 1, 4B, 4D).

Thus, Chen does not teach the step of "subsequently implanting a dopant of a second conductivity type which is different from said first conductivity type into said substrate . . . to form said dopant pockets beneath said source regions," as amended independent claim 1 recites. In fact, even if the deep N well 130 of Chen would *arguendo* be considered a source region, Chen teaches forming "n+ well 132 embedded within deep N well 130," and not "subsequently *implanting* a dopant of a second conductivity type which is different from said first conductivity type into said substrate . . . to form said dopant pockets beneath said source regions," as in the claimed invention (emphasis added).

Similarly, Gardner fails to teach or suggest all limitations of amended independent claim 1. The crux of Gardner is the formation of an asymmetrical gate oxide thickness in a channel region of a MOSFET (abstract), and not a "method of forming a plurality of dopant pockets" of flash memory cells, as in the claimed invention, much less the specific steps of amended independent claim 1.

Chen and Gardner fail to teach or suggest "implanting a dopant into said substrate through said respective substrate regions to form said dopant pockets beneath said source regions, said photoresist operating as a mask for forming said source regions and said dopant pockets, wherein said act of implanting said dopant into said substrate is carried out before said act of forming said source regions," as independent claim 12 recites. Chen specifically teaches that the n+ well 132, which would arguably correspond to the source region of the claimed invention, is a shallow layer which is "embedded within deep N well 130," which would arguably correspond to the dopant pocket of the claimed invention. (Col. 7, lines 1-5; Figure 4D). Chen also specifically teaches that *mask 710 is removed prior to* a second implant and formation of n+ well 132. (Figs. 4, 4A-4D, 6, 6D-6F, 8, and 8C-8F). Thus, Chen clearly teaches *away from* the claimed invention according to which the photoresist operates as a "mask for forming said source regions *and* said dopant pockets." (emphasis added). Accordingly, the formation of the flash structure containing *both* wells 130 and 132 could not have been carried out in the presence of photomask, since Chen explicitly teaches removal of the photomask prior to formation of the flash structure containing *both* wells 130 and 132.

Similarly, Gardner teaches the removal of photoresist 110 prior to the formation of the LDD regions 120, 122, which would arguably correspond to the dopant pockets of the claimed invention. Gardner specifically emphasizes that "photoresist 110 is stripped, and lightly doped source and drain regions 120 and 122 are implanted into substrate 102 by subjecting the structure to ion implantation of phosphorus." (Col. 4, lines 61-64). In fact, Gardner specifically notes that "[t]he ion implantation of phosphorus is done through the layer of gate oxide 104" and that "[p]olysilicon gate 112 provides an implant mask for the underlying portion of substrate 102" (col. 4, lines 66-67; col. 5, lines 1-2).

Chen and Gardner, whether considered alone or in combination, also fail to teach or suggest the limitations of independent claims 13, 19, 20 and 24. Chen and Gardner are silent about "forming a source region in between said word lines" and "subsequently implanting *boron* into said substrate in between said word lines," much less about implanting boron into said substrate "to form a boron pocket *beneath* said source region," as independent claims 13 and 19 recite. Chen teaches only that "[s]ource 112 and drain 114 regions . . . are conventionally formed by . . . implanting n-type dopants." (Col. 6, lines 55-63; Figures 1 and 4B). Chen is silent, however, about any dopant implantation subsequent to the formation of the source/drain regions and beneath the source/drain regions, much less about p-type dopant implantation, such as boron implantation, "to form a boron pocket *beneath* said source region," as independent claims 13 and 19 recite.

Gardner also fails to teach or suggest the formation of a boron pocket of a flash memory, much less "implanting boron into said substrate in between said word lines to form a boron pocket beneath said source region," as independent claims 13 and 19 recite. As noted above, the crux of Gardner is the formation of a gate structure of a MOSFET having specific dielectric materials, and not the formation of boron pockets of flash memory cells, as in the claimed invention. Chen and Gardner also fail to teach or suggest "forming a pair of gate structures which extend in a first direction over a substrate" and "altering the upper surface profile of said substrate to form alternating areas of higher substrate surface elevation and areas of lower substrate surface elevation along said first

direction and between said pair of gate structures," as independent claims 20 and 24 recite.

Second, Applicant notes that a person of ordinary skill in the art would not have been motivated "to combine Gardner with Chen so as to modify Chen's order of implants," as the Office Action asserts. (Office Action at 4). As noted above, the crux of Chen is the formation of a flash EEPROM having reduced column leakage current. Chen teaches "[a]n intermediate n+ implant immediately following the DDI implant step" to provide "an enhanced doping profile in the tunneling region, which increases the rate at which F-N tunneling occurs to erase the cells, and which increases the uniformity of F-N tunneling rates among memory cells within the array." (Abstract). Chen specifically emphasizes that "[a] thermal cycle drives the intermediate n+ implant deeper into the tunneling region." (Abstract).

On the other hand, Gardner relates to a method of "reducing hot carrier effects" by forming a gate of a MOSFET transistor having "a first material having a first dielectric constant adjacent the semiconductor substrate and a second material having a second dielectric constant adjacent the semiconductor substrate" (abstract), and not reducing column leakage current in flash EEPROMs, as in Chen. It is clear, therefore, that the Examiner has pointed to no teaching or suggestion in the prior art that would have motivated one of ordinary skill to combine and modify Chen with Gardner, as proposed by the Examiner. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 1-7, 9-14 and 16-24 is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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